Formal Verification student

Summary

Ready for an intellectual challenge that combines Mathematics and CS theory in the context of hardware development? Keep reading. In this role you will be responsible for developing mathematical proofs using model checking tools, to find RTL(Verilog) bugs or prove their absence Not in the Formal domain? No worries, we offer thorough training to learn the theory and practice directly from our team experts

Description

In this role you will be responsible for developing mathematical proofs using model checking tools, to find RTL(Verilog) bugs or prove their absence . The position is relevant for both Herzliya/ Haifa site

Key Qualifications

- Excellent graduates from leading universities
- Analytical thinking
- Highly motivated

Education & Experience

Student for B.Sc. in Computer Science and Math, Computer Engineering, Computer Science and Physics or student for M.Sc/PhD in Mathematics.

Apply here